

SEPTEMBER 2006

CAEB		Approval Date:	
Lectures/week	3 hours	Math	0%
Tutorials/week	1 hours	Basic Science	0%
Labs/week	2 hour	Complementary Studies	0%
Weeks/term	12.4	Engineering Science	60%
		Engineering Design	40%

Course description

This is an introductory course to digital systems which includes basic concepts on manual and automated digital system design. The course covers concepts on digital system design, including basic design concepts and implementation technology, number representations, synthesis of combinational and sequential logic, and the use of HDL and computer-based design tools. Prerequisites: CS 1073 or equivalent, EE 1813 recommended.

Course Content

1. Introduction: Design concepts, digital hardware, basic design loop
2. Introduction to Logic Circuits: Truth tables, logic gates, Boolean algebra, SOP and POS forms, introduction to CAD tools, introduction to a hardware description language.
3. Implementation Technology: MOSFET Switches, Overview of Standard Logic and Programmable Logic Devices.
4. Synthesis: Karnaugh maps, minimization, incomplete specifications, CAD tools and synthesis.
5. Number Representations and Basic Arithmetic: Unsigned and signed ripple-carry adders, Look ahead carry generation.
6. Combinational Circuit Building Blocks: Multiplexers, decoders, encoders, code converters, arithmetic comparison circuits, hardware description language encoding for combinational circuits.
7. Flip-flops, Registers, Counters: Basic latches, gated latches, D-flip-flops, shift registers, register files, counters, hardware description language encoding for registers.
8. Synchronous Sequential Circuits: Analysis, design steps, state assignment, Mealy and Moore state-machines and hardware description language code for state machines.
9. Register Transfer Concepts. Basic data path flow and CPU Operation.
10. Midterm test and final.

Total hours 39

Labs

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| 1. Introduction to Logic Circuits | 5. A Four-Bit Adder/Subtractor |
| 2. Introduction to the Altera's FPGA Board | 6. A Binary Counter |
| 3. Schematic capture in Quartus | |
| 4. A Hex to Seven Segment Decoder | Project (3 weeks) |

Course evaluation

Assignments	10%	Labs	19%
Tests	19%	Final	52%

Course regulations

According to new department regulations, only one deferral exam date will be scheduled. It will be the first Thursday of the next term. Student missing the regular exam date will have to submit reason in writing and will have to wait until the unique deferral exam date to write the exam.