Syllabus CMPE2213 (EE2213) – Digital Systems I

UNIVERSITY OF NEW BRUNSWICK *DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING*

SEPTEMBER 2007

CAEB		Approval Date:	
Lectures/week	3 hours	***Math***	0%
Tutorials/week	1 hours	***Basic Science***	0%
Labs/week	2 hour	***Complementary Studies***	0%
Weeks/term	12.4	***Engineering Science***	60%
		Engineering Design	40%

Course description

This is an introductory course to digital systems which includes basic concepts on manual and automated digital system design. The course covers concepts on digital system design, including basic design concepts and implementation technology, number representations, synthesis of combinational and sequential logic, and the use of HDL and computer-based design tools. Prerequisites: CS 1073 or equivalent, EE 1813 recommended.

Course Content

1. Introduction: Design concepts, digital hardware, basic design loop
2. Introduction to Logic Circuits: Truth tables, logic gates, Boolean algebra, SOP and POS forms, introduction to CAD tools, introduction to a hardware description language.
3. Implementation Technology: MOSFET Switches, Overview of Standard Logic and Programmable Logic Devices.
4. Synthesis: Karnaugh maps, minimization, incomplete specifications, CAD tools and synthesis.
5. Number Representations and Basic Arithmetic: Unsigned and signed ripple-carry adders, Look ahead carry generation.
6. Combinational Circuit Building Blocks: Multiplexers, decoders, encoders, code converters, arithmetic comparison circuits, hardware description language encoding for combinational circuits.
7. Flip-flops, Registers, Counters: Basic latchs, gated latchs, D-flip-flops, shift registers, register files, counters, hardware description language encoding for registers.
8. Synchronous Sequential Circuits: Analysis, design steps, state assignment, Mealy and Moore state-machines and hardware description language code for state machines.
9. Register Transfer Concepts. Basic data path flow and CPU Operation.

Total hours 39

Labs/Project

1. Introduction to Logic Circuits
2. Introduction to the Altera's FPGA Board
3. Schematic capture in Quartus

1 Project (3 weeks)

4. A Hex to Seven Segment Decoder
5. A Four-Bit Adder/Subtractor
6. Coder/Decoders

7 A Binary Counter

Course evaluation

Assignments	10%	Labs	15%
Tests	20%	Project	5%
Final	50%		

Course regulations

University regulations on deferred exams are described in Section B – V. Examination, Standing and Promotion, C. Deferred Examinations of the current Undergraduate Calendar.
All deferred exams in courses offered by the Department of Electrical and Computer Engineering are scheduled to be written on the fourth day of classes in the following term. There are no exceptions.