A Reconfigurable Four-Channel Transceiver Testbed with Signalling-Wavelength-Spaced Antennas under Centralized FPGA Control

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Abstract

We propose a novel software defined radio implementation of a four-channel transceiver testbed with signalling-wavelength-spaced antennas. The radio frequency (RF) side of the system will be implemented using commercial off the shelf (COTS) products, whereas the baseband processing portion of the system will be implemented on a pair of Altera Stratix II EP2S180 development boards with high-speed Analog Devices analog-to-digital converter (ADC) daughter boards. The FPGA will be used to implement DSP algorithms and to affect centralized control over the entire system. A goal is to create a testbed for algorithms and radio channel measurements.

1. Introduction

The goal of this project is to develop a centrally controlled, reconfigurable, four channel radio testbed which takes advantage of space-time techniques as well as new antenna spacing theories. This testbed will be used to make radio channel measurements, and to enable researchers to take advantage of the rapid prototyping capabilities of field programmable gate array (FPGA) technology, in order to better investigate their hypotheses.

The system will be comprised of four transmitters and four receivers. A space-time receiver will be implemented in order to distinguish amongst users and provide diversity gain. The receive antennas will be separated by one signalling wavelength, in order to take advantage of signalling wavelength antenna placement (SWAP) gain described by Zhu et al. [1] and the chip length by Yanikomeroglu et al. [2]. We may use the 2.4 GHz industrial, scientific, and medical (ISM) band for this project with a 10 Mbps data rate. Based on signalling-wavelength spaced antennas, this corresponds to receiver inter-antenna spacing of 60 meters (with 100% excess bandwidth).

In order to allow for more flexibility and to avoid having to create our own RF front end, we have chosen suitable high-end radio receivers with 10.7 MHz intermediate frequency (IF) outputs, automatic gain control, and phase locking capabilities to interface to the system.

2. System overview/requirements

The system is composed of three main sub-systems: the transmit side, the receive side, and central FPGA baseband processing system. In order to achieve the requirements of a four transmitter and a four receiver multiple-input multiple-output (MIMO) array, for use in the 2.4 GHz ISM band, several basic requirements must be met. The FPGA must support at least four ADCs of appropriate frequency and resolution. As well, a space-time receiver structure with signalling-wavelength spaced antennas will be used to isolate individual user data streams and take advantage of diversity and SWAP gain.

At the center of the system sits a pair of Altera Stratix II DSP Development boards which will be responsible for generating the signal to be transmitted, as well as processing the received baseband signal. The FPGAs will also be used to provide high-level control over the entire system from a central location, providing the means to implement more advanced tests.

3. Transmit side

The transmit side of the system consists of four identical transmitter circuits. Each transmitter represents a single user in the system, enabling our system to simulate up to four simultaneous users at a time.

In order to generate known digital signals for use as training sequences, eight linear recursive sequence (LRS) generators with different tap configurations will be used to generate a pair of inphase (I) and quadrature (Q) signals for each user. The generation of these signals will be performed by one of the FPGAs and output using eight of the general purpose input/output (GPIO) pins on the development board.

Once the digital signals have been created and output from the FPGA, all that is left is to modulate the data onto

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the 2.4 GHz carrier waveform and radiate it via the transmit antennas. To achieve modulation, we have chosen to use four Hittite HMC497lP4 vector modulator demo boards coupled with an Aeroflex 2025 signal generator to provide the carrier sinusoid. However, in order to interface the eight FPGA GPIO pins to the Hittite vector modulators, some voltage translation is required. Specifically, the FPGA board outputs 0-3.3V [3], whereas the Hittite vector modulator requires a 1.6Vpp input with a 1.5V DC offset. To achieve the required translation, a custom printed circuit board (PCB) has been designed and is in the process of fabrication.

A simplified block diagram of an individual transmitter is shown in Figure 1 below.

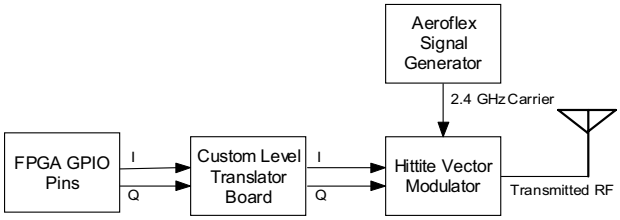

Figure 1. Transmitter structure

The position of each of the transmit antennas will be midway between each of the receive antennas. That is, approximately 60 meters away from the center of the array.

4. Receive side

The receive side of the system consists of four identical receiver circuits. These receivers provide four channels of incoming RF data to be processed by the system. In order to simplify the RF front-end design for our receivers, we are using four AOR AR5000A+3 wide band all mode receivers. The RF signals which arrive at each of the four receive antennas will be down-converted using the AOR radios, which provide a 10 MHz IF output centered at 10.7 MHz.

IF sampling of the incoming data will be performed using four Analog Devices AD6645/PCB daughter boards which have special headers allocated to them on the Altera Stratix II DSP Development Board. This allows two channels of incoming data to be received by each Altera Development Board. The sampling rate of the ADCs will have to be greater than 31.4 MHz in order to satisfy Nyquist criterion. The conversion clock will be provided by the FPGAs.

To avoid synchronization issues, each of the four AOR radios as well as the two Altera FPGA boards will be locked to a common 10 MHz reference. Automatic gain control (AGC) will also be provided by the AOR radios.

Figure 2 illustrates the basic structure of each of the four receivers.

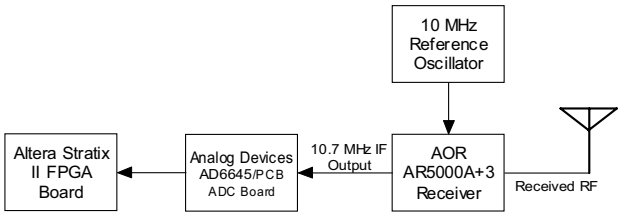

Figure 2. Receiver structure

5. Baseband processing

Once the IF signal has been sampled, a 5.7-15.7 MHz bandpass finite impulse response (FIR) filter, in the FPGA, will remove any unwanted spectrum. A space-time (ST) receiver, using an adaptive algorithm, will then be implemented on the FPGA. The ST receiver will enable the recovery of the transmitted signals for each user. In order to achieve this, the array will consist of four groups of four adaptive filters. Each filter from each of the groups of four will connect to a different receive antenna input, and each particular group will be trained to isolate the signal of only one user in the system. The outputs of each of the four adaptive filters in a particular group will then be combined to average the signals from the four antennas. This limits the number of users in a linear system to sixteen, but will provide diversity gain over the single antenna case. The ST receiver structure which will be implemented for this system is described by Paulraj et al. [4].

6. Centralized control

In order to achieve central control over the entire functionality of the system, the FPGAs need to be able to communicate with each of the individual components. The first step in designing this control system was to select components which can be remotely controlled via RS-232C. Using the RS-232C interface on the Altera FPGAs, coupled with a BlackBox code operated switch, it is possible to uniquely address each of the components. This enables remote access to all the features of the radios and the signal generators. Since we also control the baseband transmit and receive functions directly via the FPGA, this provides complete control over the system. Advanced testing such as swept frequency, for instance, could be achieved by simply sweeping the tuned frequency of the radio receivers across the frequency spectrum of interest. Figure 3 illustrates the baseband side of the system and how it interacts with and controls the rest of the hardware in the system.

There are several issues which arise due to the fact that our antenna array is spread over such a large area. Firstly, the location of each of the components becomes important. Since the rate of the incoming signal to both

the receive and transmit antennas is 2.4 GHz, there would be a great deal of attenuation over 60 meters of coaxial cable. To avoid this problem, both the AOR radios and the Hittite Vector Modulator Boards will be situated close to their respective receive/transmit antennas. Thus, the signals traveling through the 60 meter run of coax cable will be at the IF frequency of 10.7 MHz which, coupled with low loss cabling, should be acceptable.

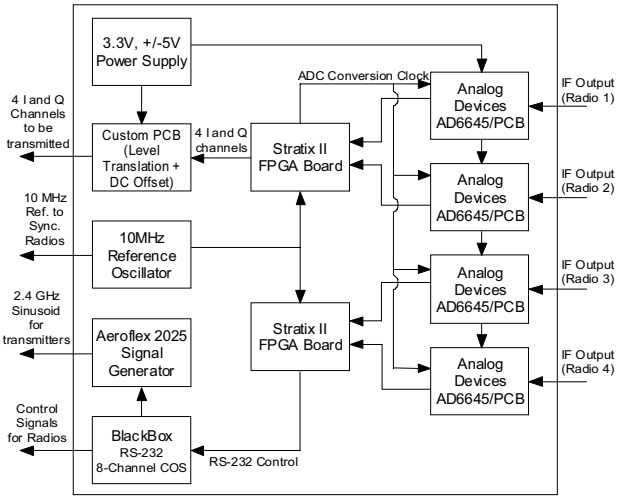

Figure 3. Baseband processing architecture

The second issue derives from the first, and our desire to control the array centrally. In order to synchronize all the AOR radios, a 10 MHz reference signal must be shared amongst them. Furthermore, centralized control over these radios requires that each has a RS-232C connection to the central hub. This translates to 2x60 meter runs of coax, plus 1x60 meter run of RS-232C cable per receive antenna. Combined with the cabling required for the I, Q, and 2.4 GHz reference signals sent to each transmit antenna (3x60 meters of coax), the grand total comes to 1200 meters of coax plus 240 meters of RS-232 cabling.

Figure 4 shows the topology of the array along with the signals which are sent amongst the various components.

7. Progress to date and future work

To date, all of the required hardware pieces have been selected and most have been acquired or ordered. The LRS generator circuits for the transmitters have been designed and simulated. As well, the custom interface board to connect the GPIO pins of the Stratix II FPGA board to the Hittite vector modulator has been designed and is in the process of being manufactured.

Since the receiver and transmitter portions of the system are made primarily of COTS components, it should only be a matter of interconnecting and pieces and verifying that they are working correctly. This leaves the baseband processing system and the centralized control system left to be implemented.

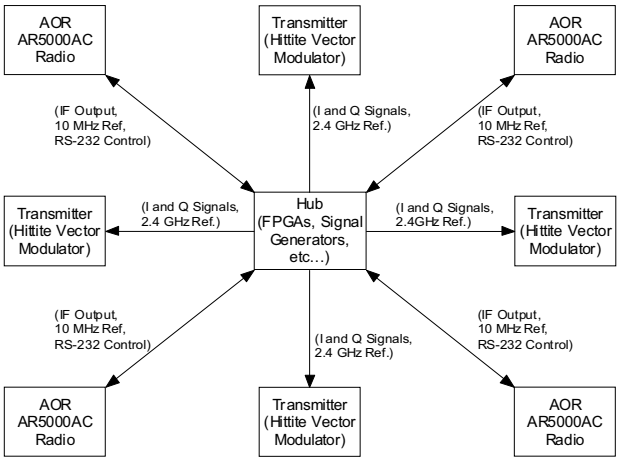

Figure 4. System topology

Once the implementation and testing phase is complete, the system will be ready for use in taking field measurements for characterization of the radio channel.

8. Acknowledgement

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9. References

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