THE 80C188XL MICROPROCESSOR SYSTEM

EE3232 DIGITAL SYSTEMS III
CLASS NOTES CHAPTER 2

Department of Electrical Engineering
University of New Brunswick

 January 14, 2000

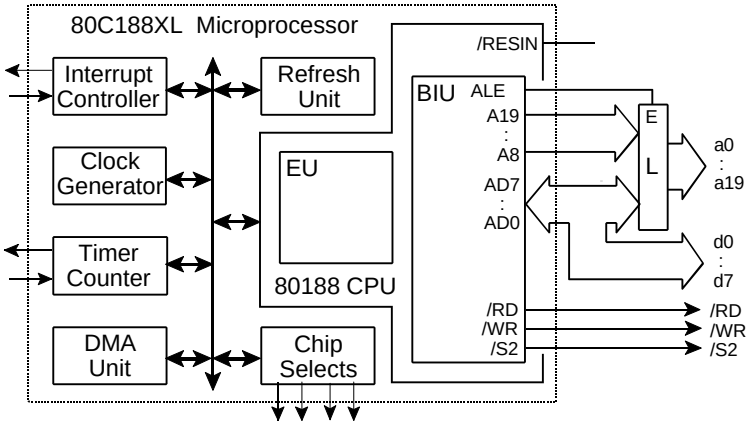
SUMMARY

- The 80C188XL microprocessor.
- The 80188 core CPU subsystem.
- The 80188 execution unit or EU.
- The 80188 flag register or PSW.
- The 80188 bus interface unit or BIU.
- Addressing modes of the 80188.
- Memory addressing supported by the 80188.
- External memory in the 80C188XL microprocessor system.
- External IO in the 80C188XL microprocessor system.
- Control bus decoding.

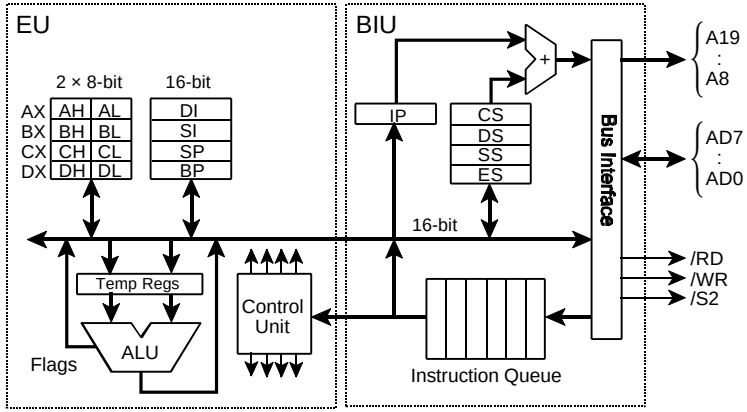
THE 80C188XL MICROPROCESSOR

- 20-bit address bus and 8-bit data bus.
- Address and data share the AD0 - AD7 pins.

THE 80C188XL MICROPROCESSOR (CONT'D)



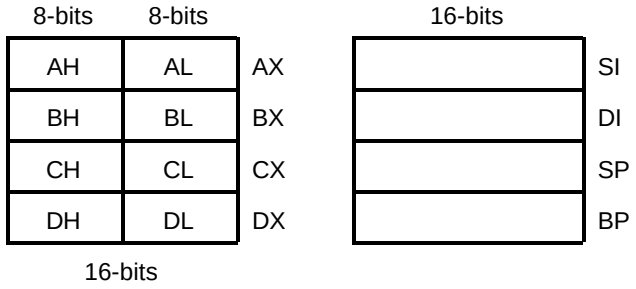
THE 80188 CORE CPU SUBSYSTEM



16 - bit ALU
20 - bit Address Bus
16 - bit Internal Bus and Registers
8 - bit External Data Bus

The 80188 Execution Unit or EU

- The EU consists of an instruction decoder, a control unit, a 16-bit ALU, a flag register and the user registers :



THE 80188 FLAG REGISTER OR PSW

ALU and Processor Flags		
CF	**Carry**	Set if there is a carry/borrow out of the MSB of the ALU result.
PF	**Parity**	Set if the result has an even number of 1's.
AF	**Aux Carry**	Set if there is a carry/borrow out of bit-3 of the ALU result.
ZF	**Zero**	Set if the result is zero.
SF	**Sign**	Set if the MSB of the result = 1.
OF	**Overflow**	Set if the ***signed*** result won't fit into n-bits.
TF	**Trap**	Enables the single stepping interrupt if set.
IF	**Interrupt**	Enables hardware interrupts if set.
DF	**Direction**	Controls the direction of string operations.

THE 80188 BUS INTERFACE UNIT OR BIU

- ALE = 1 when AD0 - AD7, A8 - A19 contain addresses.
- Data appears at AD0 - AD7 when /RD = 0 or /WR = 0.
- The BIU generates external addresses and control signals.
- Instructions fetched from memory are placed in a first-in first-out ***instruction queue*** (instead of the Instruction Register).
- The queue allows the BIU to fetch instructions at the same time that the EU is executing a previous instruction.

THE 80188 BUS INTERFACE UNIT OR BIU (CONT'D)

- The 20-bit address generated at the AD_0 - AD_7 , A_8 - A_{19} pins is referred to as the ***physical address***, or PA.
- 20-bit physical addresses are generated in the BIU as,

  PA = EA + 16*SA = EA + SA << 4

- EA = ***effective address***, is always contained in one of the 16-bit registers : { AX, BX, CX, DX, SI, DI, SP, or BP } or IP.
- SA = ***segment address***, is always contained in one of the 16-bit segment registers : { CS, DS, ES or SS }.
- The notation ***SA:EA*** is used to denote a PA.
- What PA corresponds to the address 2A00:5680H?

ADDRESSING MODES OF THE 80188

- A typical instruction has the form,

  OPCODE **left_operand**, **right_operand**

- The operands may appear in the following combinations,

left_operand	right_operand
reg	reg
reg	immediate data
mem	immediate data
reg	mem
mem	reg

reg ∈ { AX, AL, AH, BX, BL, BH, CX, CL, CH, DX, DL, DH, SI, DI, SP, BP }
mem ∈ { a supported memory addressing mode }

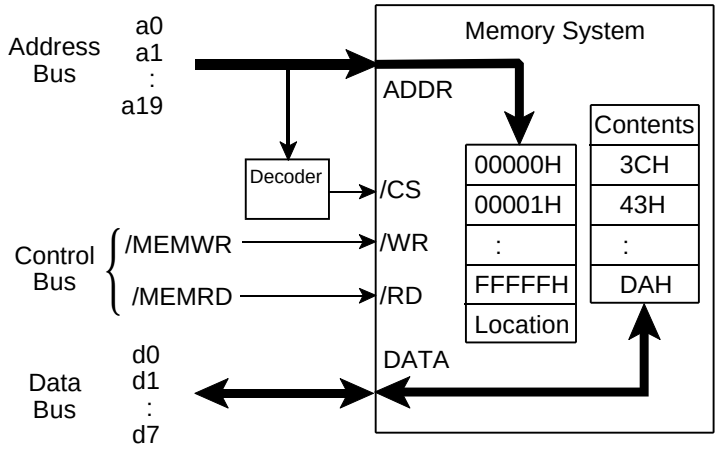
NOTE : memory to memory transfers are ***not*** supported !

MEMORY ADDRESSING SUPPORTED BY THE 80188

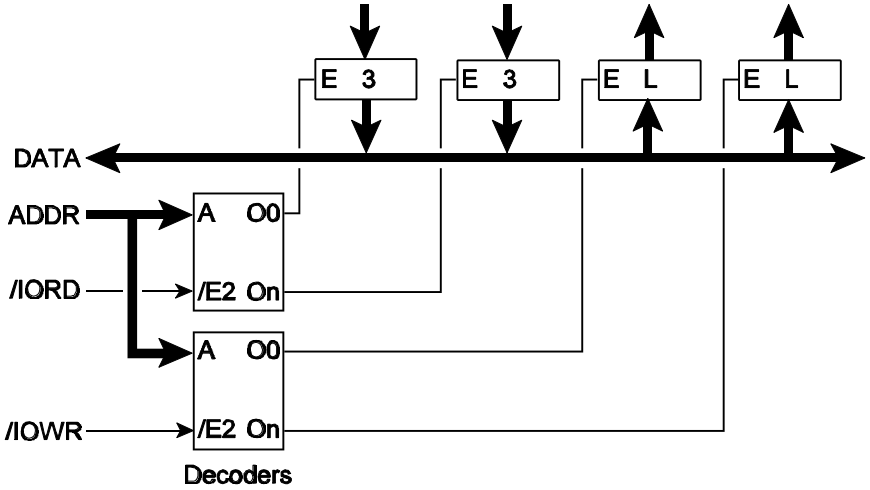
mem	Addressing	Seg Reg*
[constant]	Direct	ds
[si], [di], [bx]	Register Indirect	ds
[si + const]	Relative	ds
[di + const]		ds
[bx + const]		ds
[bx + si]		ds
[bx + di]		ds
[bx + si + const]		ds
[bx + di + const]		ds
[bp + const]		ss
[bp + si]		ss
[bp + di]		ss
[bp + si + const]		ss
[bp + di + const]		ss

*Default segment register used to generate a PA.

EXTERNAL MEMORY IN AN 80C188XL SYSTEM



EXTERNAL IO IN AN 80C188XL SYSTEM



CONTROL BUS DECODING

- /S2 = '0' ➜ IO bus cycle.
- /S2 = '1' ➜ memory bus cycle.
- /RD = '0' ➜ transfers into CPU.
- /WR = '0' ➜ transfers from CPU.