ANALOG OUTPUT SYSTEMS

EE3232 DIGITAL SYSTEMS III
CLASS NOTES CHAPTER 7

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SUMMARY

- Objectives.
- Quantization and coding.
- Op-amp circuits.
- DAC components.
- DAC transfer functions.
- Weighted resister DAC.
- R-2R ladder DAC.
- DAC coding (binary, complementary binary, offset binary, complementary offset binary, two's complement).
- DAC specifications.
- DAC calibration.
- Interfacing m-bit DAC's to an n-bit system bus.
- Interfacing the DAC667.
- Sample hold devices.
- Multiplexed sample hold devices.
- Multi-channel analog output systems.

OBJECTIVES

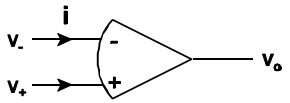
- Using basic components construct weighted resistor and R-2R ladder digital to analog converters, or DAC's.
- To relate DAC hardware and DAC coding.
- Develop H/W and S/W to convert data from one coding to another.
- To develop H/W and S/W for interfacing DAC's to a system bus.
- To develop a procedure and circuit for nulling DAC gain and offset errors.
- To develop the H/W and S/W for interfacing multi-channel output systems to a system bus.

QUANTIZATION AND CODING

- Physical phenomena are ***continuous*** or analog in nature.
- To interact with the physical world we need to transform
  - From the ***discrete domain*** of the computer
  - To the ***continuous domain*** of the real world.
- The transformation uses ***digital to analog converters***.
- Only a finite number of values for the physical phenomena can be uniquely represented by an n-bit register.
- The physical phenomena is said to be ***quantized*** to n-bits, i.e., there are 2^n quanta.
- Each quanta is related to the physical world by some form of coding, i.e., binary, 2's complement ...

OP-AMP CIRCUITS

- The fundamental building block of a DAC is the ***op-amp***.
- ***Op-amps*** : characterized by very large gain and very high input impedance.

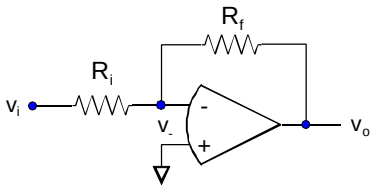


$$v_o = K(v_+ - v_-)$$

$$K \rightarrow \infty, \quad i \rightarrow 0$$

OP-AMP CIRCUITS (CONT'D)

- An op-amp configured as a (negative gain) ***amplifier***. v_o ?

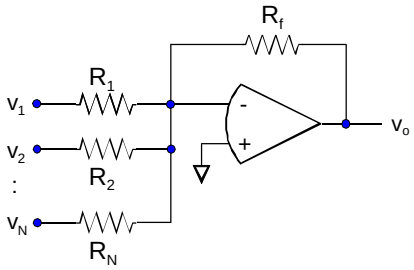


$$\frac{v_i - v_-}{R_i} = \frac{v_- - v_o}{R_f}, \quad v_- \approx 0$$

$$v_o = -\frac{R_f}{R_i} v_i$$

OP-AMP CIRCUITS (CONT'D)

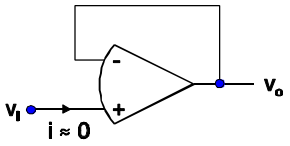
- An op-amp configured as a ***summer***. v_o ?



$$v_o = -\frac{R_f}{R_1} v_1 - \frac{R_f}{R_1} v_2 \ldots - \frac{R_f}{R_N} v_N$$

OP-AMP CIRCUITS (CONT'D)

- An op-amp configured as a high (input) impedance ***unity gain amplifier***. v_o ?

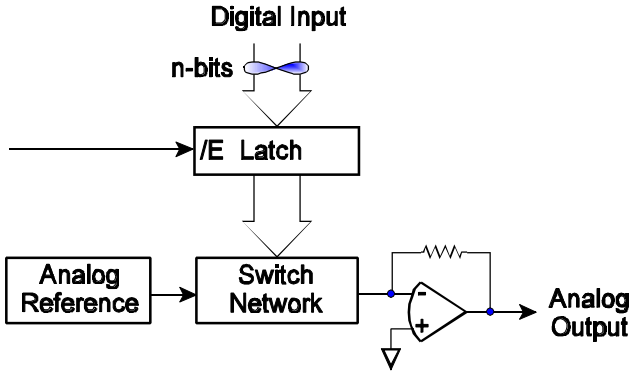


$$v_o = v_i$$

DAC COMPONENTS

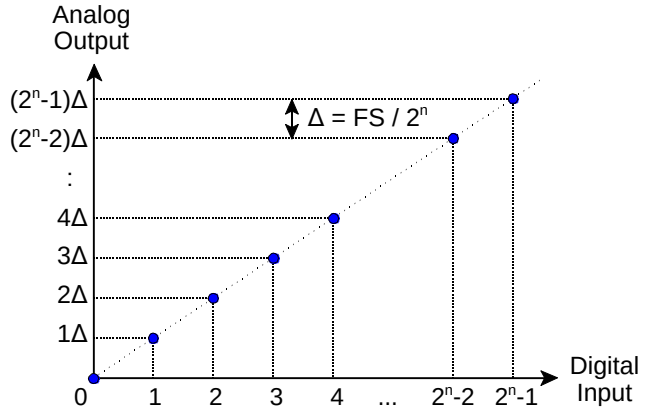
- A DAC consists of :

1. A stable analog reference voltage (or current),
2. A switching network of resistors (or capacitors) and
3. An op-amp for summing voltages or currents.
4. Latch to hold the digital input.



DAC Transfer Functions

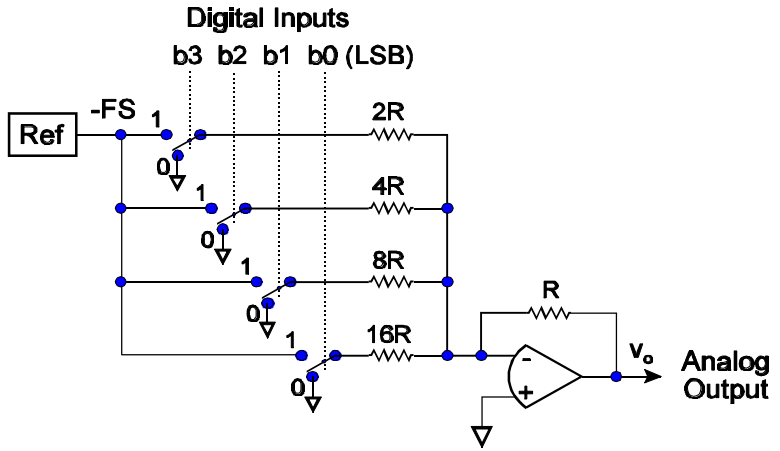
- The DC transfer function of a (straight binary) DAC.
- FS : The full scale analog voltage (the reference voltage).



DAC Transfer Functions (cont'd)

- ***DAC resolution*** : refers to the change in DAC output for a change in the least significant bit, LSB, of the input.
- Resolution may be expressed as a ratio or percentage.
- Resolution of a 10-bit DAC : 1 part in 1024 or 0.0977%.
- Resolution of a 14-bit DAC : 1 part in 16384 or 0.00610%.

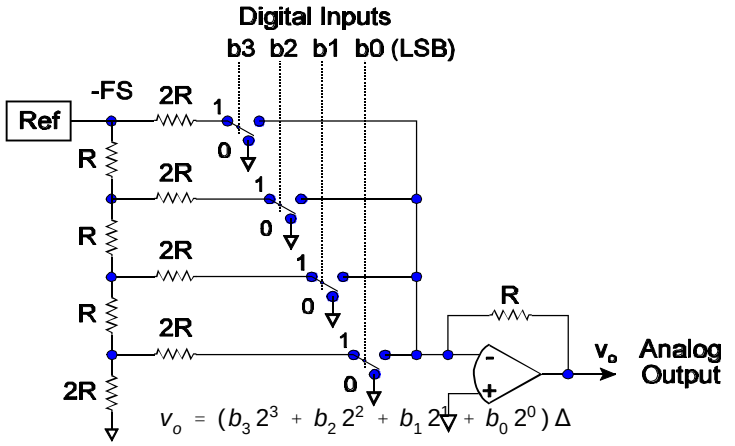
Weighted Resistor (Straight Binary) DAC



$$v_o = (b_3 2^3 + b_2 2^2 + b_1 2^1 + b_0 2^0)\,\Delta$$

$$= B\Delta\,, \quad \Delta = \frac{FS}{16}\,, \quad B \text{ unsigned.}$$

R-2R Ladder (Straight Binary) DAC



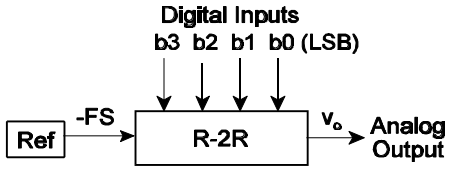
$$v_o = (b_3 2^3 + b_2 2^2 + b_1 2^1 + b_0 2^0)\,\Delta$$

$$= B\Delta\,, \quad \Delta = \frac{FS}{16}\,, \quad B \text{ unsigned.}$$

DAC CODING

- How do choices in H/W affect coding ?
- Straight Binary (Unipolar).
- Complementary Binary (Unipolar).
- Offset Binary (Bipolar).
- Complementary Offset Binary (Bipolar).
- Two's Complement (Bipolar).

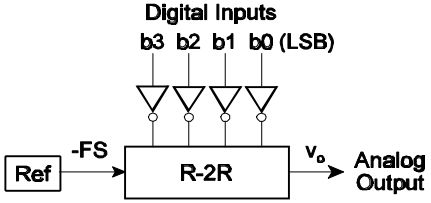
STRAIGHT BINARY (UNIPOLAR) CODING



$$v_o = (b_{n-1}2^{n-1} + b_{n-2}2^{n-2} + \ldots + b_1 2^1 + b_0 2^0)\Delta$$

$$= B\Delta, \quad \Delta = \frac{FS}{2^n}, \quad B \text{ unsigned.}$$

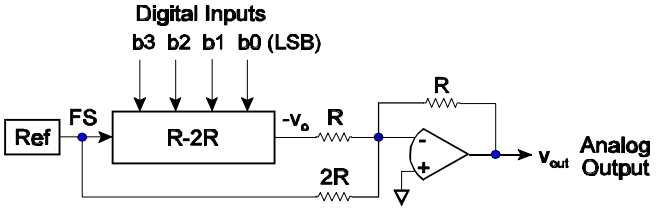
COMPLEMENTARY BINARY (UNIPOLAR) CODING



$$v_o = (\overline{b_{n-1}}2^{n-1} + \overline{b_{n-2}}2^{n-2} + \ldots + \overline{b_1}2^1 + \overline{b_0}2^0)\Delta$$

$$= \overline{B}\Delta, \quad \Delta = \frac{FS}{2^n}, \quad B \text{ unsigned.}$$

OFFSET BINARY (BIPOLAR) CODING

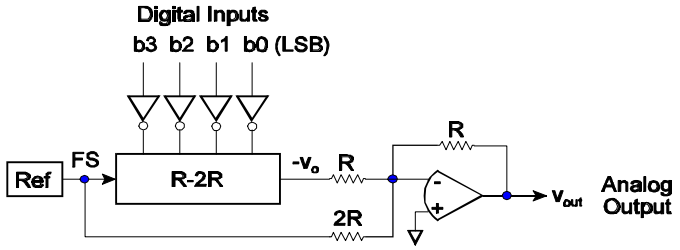


- For an n-bit DAC,

$$v_{out} = (b_{n-1}2^{n-1} + b_{n-2}2^{n-2} + \ldots + b_1 2^1 + b_0 2^0)\Delta - \frac{FS}{2}$$

$$= B\Delta - \frac{FS}{2}, \quad \Delta = \frac{FS}{2^n}, \quad B \text{ unsigned.}$$

COMPLEMENTARY OFFSET BINARY (BIPOLAR) CODING

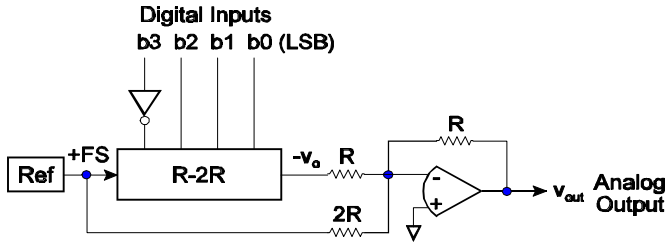


- For an n-bit DAC,

$$v_{out} = (\overline{b_{n-1}}2^{n-1} + \overline{b_{n-2}}2^{n-2} + \ldots + \overline{b_1}2^1 + \overline{b_0}2^0)\Delta - \frac{FS}{2}$$

$$= \overline{B}\Delta - \frac{FS}{2}, \quad \Delta = \frac{FS}{2^n}, \quad B \text{ unsigned.}$$

TWO'S COMPLEMENT (BIPOLAR) CODING



- For an n-bit DAC,

$$v_{out} = (\overline{b_{n-1}}\,2^{n-1} + b_{n-2}\,2^{n-2} + \ldots + b_1\,2^1 + b_0\,2^0)\,\Delta - \frac{FS}{2}$$

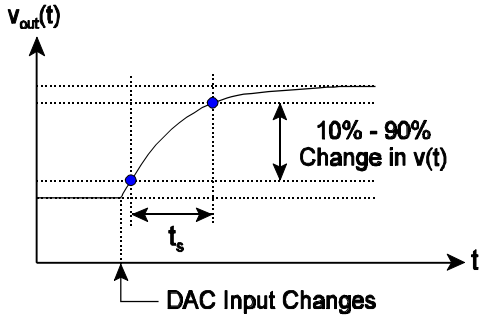
$$= B\Delta\,, \quad \Delta = \frac{FS}{2^n}\,, \quad B \text{ signed integer.}$$

BIPOLAR DAC CODING SUMMARY

Digital Coding			Analog Value		
Offset Binary	**Complementary Offset Binary**	**Two's Complement**			
0000 0000 0000	1111 1111 1111	1000 0000 0000	-10 + 0Δ =	10 - 4096Δ =	-2048Δ
0000 0000 0001	1111 1111 1110	1000 0000 0001	-10 + 1Δ =	10 - 4095Δ =	-2047Δ
0000 0000 0010	1111 1111 1101	1000 0000 0010	-10 + 2Δ =	10 - 4094Δ =	-2046Δ
:	:	:	:	:	:
0011 1111 1111	1100 0000 0000	1011 1111 1111	-10 + 1023Δ =	10 - 3073Δ =	-1025Δ
0100 0000 0000	1011 1111 1111	1100 0000 0000	-10 + 1024Δ =	10 - 3072Δ =	-1024Δ
0100 0000 0001	1011 1111 1110	1100 0000 0001	-10 + 1025Δ =	10 - 3071Δ =	-1023Δ
:	:	:	:	:	:
0111 1111 1111	1000 0000 0000	1111 1111 1111	-10 + 2047Δ =	10 - 2049Δ =	-1Δ
1000 0000 0000	0111 1111 1111	0000 0000 0000	-10 + 2048Δ =	10 - 2048Δ =	0
1000 0000 0001	0111 1111 1110	0000 0000 0001	-10 + 2049Δ =	10 - 2047Δ =	1Δ
:	:	:	:	:	:
1011 1111 1111	0100 0000 0000	0011 1111 1111	-10 + 3071Δ =	10 - 1025Δ =	1023Δ
1100 0000 0000	0011 1111 1111	0100 0000 0000	-10 + 3072Δ =	10 - 1024Δ =	1024Δ
1100 0000 0001	0011 1111 1110	0100 0000 0001	-10 + 3073Δ =	10 - 1023Δ =	1025Δ
:	:	:	:	:	:
1111 1111 1101	0000 0000 0010	0111 1111 1101	-10 + 4093Δ =	10 - 3Δ =	2045Δ
1111 1111 1110	0000 0000 0001	0111 1111 1110	-10 + 4094Δ =	10 - 2Δ =	2046Δ
1111 1111 1111	0000 0000 0000	0111 1111 1111	-10 + 4095Δ =	10 - 1Δ =	2047Δ

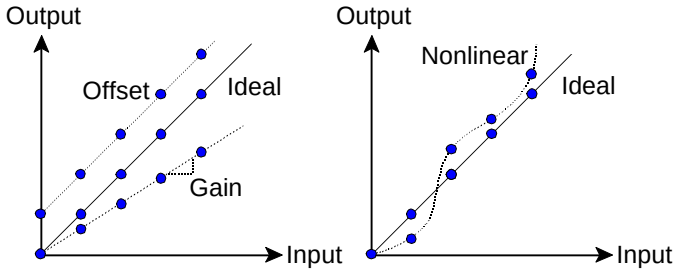
DAC SPECIFICATIONS

- ***DAC Settling Time*** : t_s, is the (maximum) time required for the analog output of the DAC to settle (within usually 90% of the expected change) when the DAC input changes.



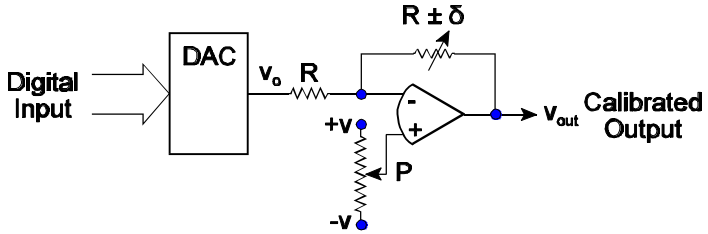
DAC SPECIFICATIONS (CONT'D)

- Real DAC's are characterized by various of phenomena that cause deviations from an ideal DAC,
  - Offset Error,
  - Scale Factor or Gain Error,
  - Nonlinearity Error.



DAC CALIBRATION

- Upper bounds on errors are given in device specs.
- If nonlinear errors are negligible then the offset and gain errors may be zeroed using the circuit and steps below.
-

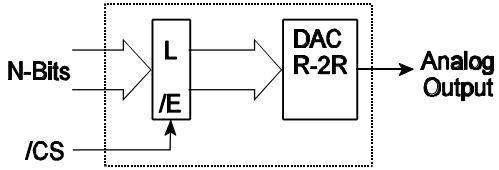


- Apply Digital Input for $v_o = 0$ ideally. Adjust P until $v_{out} = 0$.
- Apply Digital Input for $v_o = v_{max}$ ideally. Adjust δ until $v_{out} = v_{max}$.

INTERFACING M-BIT DAC'S TO AN N-BIT DATA BUS

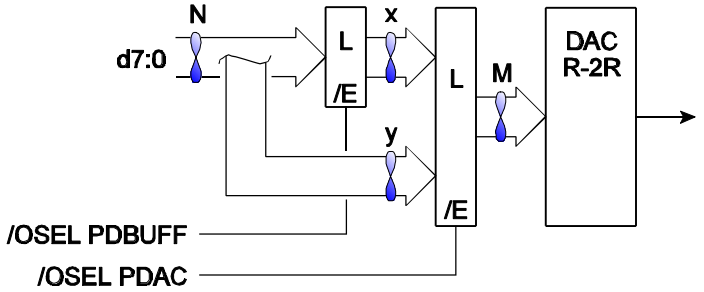
Case (i) M ≤ N

- The DAC is interfaced to a parallel output port.
- Many DAC's have built-in latches, allowing a direct interface to a system bus.
- The software interface should ensure that time between writing new values to the DAC is > the DAC settling time.

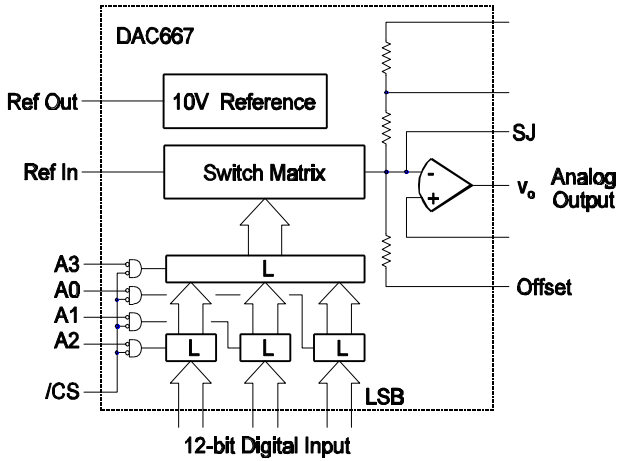


Case (ii) M > N

- Glitches at the DAC output are eliminated if all m-bits are transferred to the DAC simultaneously.
- Requires a ***double bufferred*** configuration (when M > N).
- Write x-bits to DBUFF first then write y-bits to DAC.



INTERFACING THE DAC667

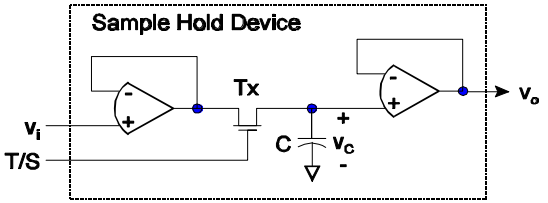


INTERFACING THE DAC667 (CONT'D)

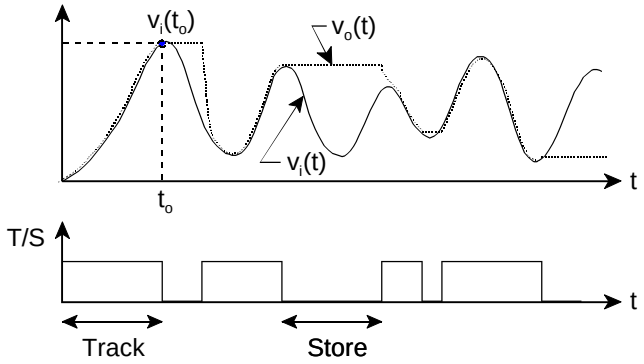
- Show how to interface the DAC667 to a system bus such that a word is transferred to the DAC as follows,
  - A write to PortA latches the 8-MSB's of the 12-bit data sent to the DAC (in a double buffer).
  - A write to PortB latches the 4-LSB's (left justified) and simultaneously loads the 8-MSB's into the DAC.
- The DAC is configured for unipolar +5 FS operation.
- Refer to the data sheets for the DAC667 in your Lab Manual.

SAMPLE HOLD OR SH DEVICES

- Analogous to an ***analog*** flip flop.

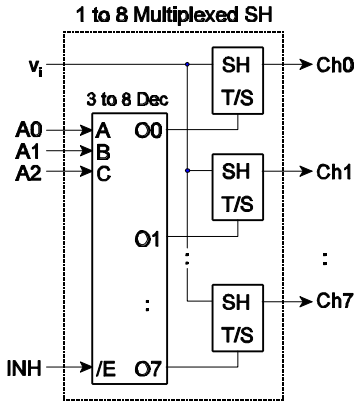


- SH Operation
  - When T/S = '1', Tx is ON ∴ $v_o(t) = v_i(t)$. $v_o(t)$ is said to track or sample $v_i(t)$.
  - When T/S = '0', at $t = t_0$, Tx is OFF ∴ $v_o(t) = v_C(t) = v_i(t_0)$. $v_o(t)$ is said to store or hold the value $v_i(t_0)$.

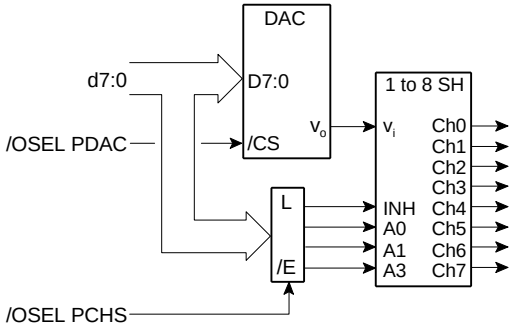


MULTIPLEXED SAMPLE HOLD DEVICES

- To store (or hold) a new analog value at Ch y
  - Activate INH ← '1' ; (Initially)
  - Apply channel number, y, to A2:0 ;
  - INH ← '0' ;
  - Ch y now tracks v_i .
  - Activate INH ← '1' ;
  - Ch y holds value.



MULTI-CHANNEL ANALOG OUTPUT SYSTEMS



- Operation,
  - Write INH = active '1' to port PCHS.
  - Write data to port PDAC.
  - Write SH channel number, y, to port PCHS.
  - Write INH = inactive '0' to port PCHS. (Ch y tracks v_o)