PROGRAMMABLE TIMERS / COUNTERS

EE3232 DIGITAL SYSTEMS III
CLASS NOTES CHAPTER 10

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SUMMARY

- Programmable interval timers, PIT's.
- The 80C188XL timers.
- The 80C188XL timers - TIMER2.
- The 80C188XL timers - TIMER0 and TIMER1.
- S/W interface for the 80C188XL timers.
- The 82C54A PIT - internal architecture.
- Read-write operation table for the 82C54A.
- Programmers model for the 82C54A PIT.
- Operation modes of the 82C54A.
- 82C54A programming example.
- Real time clocks.
- Watchdog timers.

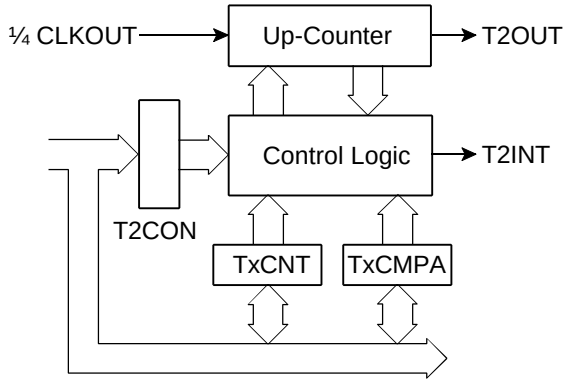
PROGRAMMABLE INTERVAL TIMERS OR PIT'S

- PIT's are peripherals dedicated for generating precisely timed periodic and aperiodic signals.
- Applications : real time clocks, baud rate generators, event counters, one shots, noise generators, periodic interrupts ...
- Examples :
  - The built-in 80C188XL timers,
  - The 82C54A timers,
  - The MC146818 real time clock (year-month-day-hour-min-sec)

THE 80C188XL TIMERS

- Three binary up-counters, **Timer0**, **Timer1**, **Timer2**, count UP to the "maximum compare value".
- Write to 16-bit port TxCON to program the mode of operation and to enable/disable counting.
- Read or write "on-the-fly" the 16-bit port, TxCNT, (the present value of the count).
- The "maximum compare value" is read / written at the 16-bit port, TxCMPA (TxCMPB).
- **Timer2** is clocked internally at 0.25*CPU clock frequency.
- **Timer2** is used primarily as a free running clock or as a pre-scaler for Timers 0 and 1.

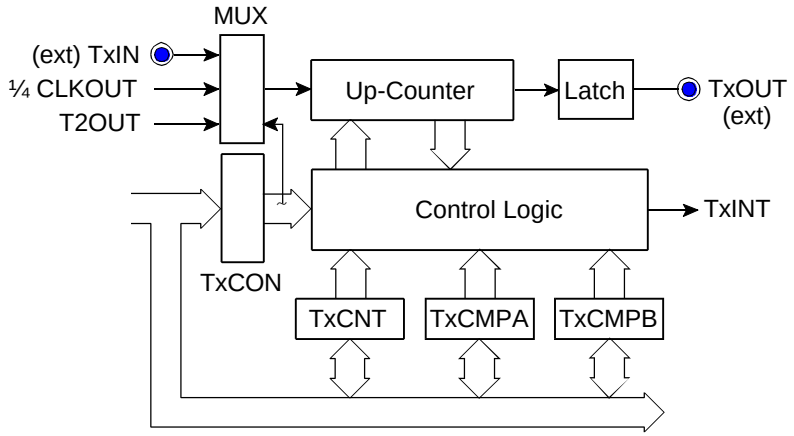
THE 80C188XL TIMERS - TIMER2



T2CON

EN	INH	INT	0	0	0	0	0	0	0	MC	0	0	0	0	CONT

THE 80C188XL TIMERS - TIMER0 AND TIMER 1



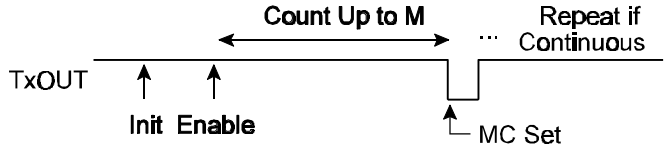
TxCON

EN	INH	INT	0	0	0	0	0	0	0	MC	0	P	EXT	ALT	CONT

S/W INTERFACE FOR THE 80C188XL INTERNAL TIMERS

Timer Initialization

- Disable counter - write 0x4000 to TxCON.
- Initialize count - write N to TxCNT.
- Initialize maximum compare value - write M to TxCPMA/B.
- Enable counter - write to TxCON

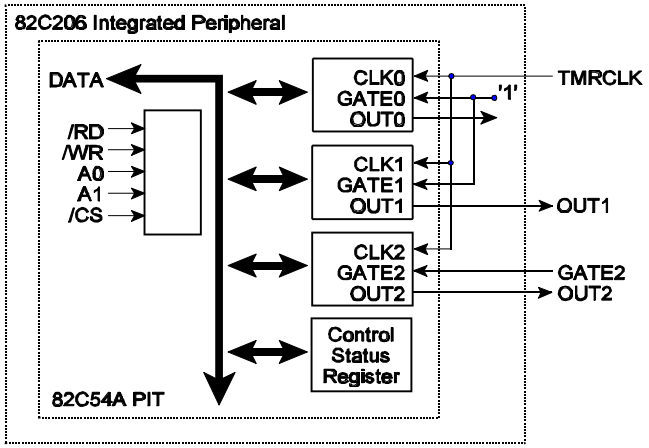


During Timer Operation

- Poll MC until MC == '1' (i.e., TxCNT == TxCMPA/B),
  Then write '0' to MC bit (to clear MC).
- Read or re-write TxCNT “on-the-fly”.

THE 82C54A PIT - INTERNAL ARCHITECTURE

- Three (8-bit or 16-bit) internal counting elements.
- Each counting element may be programmed separately.
- Count / status of each counter may be latched and read.



READ - WRITE OPERATION TABLE OF THE 82C54A

/CS	/RD	/WR	A1	A0	Operation
0	1	0	0	0	Write to Counter 0
0	1	0	0	1	Write to Counter 1
0	1	0	1	0	Write to Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	Read from Status Register
1	x	x	x	x	No Operation (3-state)
0	1	1	x	x	No Operation (3-state)

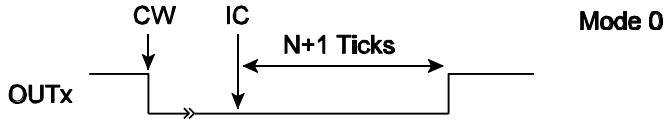
PROGRAMMERS MODEL FOR THE 8254 PIT

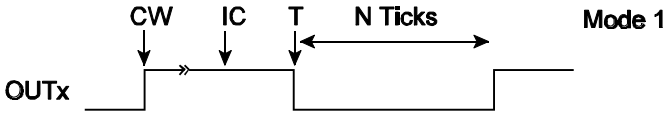
SC1 SC0 D7 D6		RW1 RW0 D5 D4		M2 M1 M0 D3 D2 D1		BCD D0		
0 0 0 1 1 0	Select counter 0 Select counter 1 Select counter 2	0 1 1 0 1 1	Read/write LSB only Read/write MSB only Read/write LSB then MSB Counter Size 8 / 16 Bits	0 0 0 0 0 1 x 1 0 x 1 1 1 0 0 1 0 1	Mode 0 Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	0 1	16-bit binary 4-decade BCD	Standard
0 0 0 1 1 0	Latch counter 0 Latch counter 1 Latch counter 2	0 0	Counter Latch Command	x x x	Don't care	x	Don't care	Counter Latch
					Select Counter			
1 1	Read-back command	0 0 0 1 1 0 1 1	Latch count & status* Latch count Latch status* No operation	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	none 0 1 0, 1 2 0, 2 1, 2 1, 2, 3	0	Must be 0	Read-back

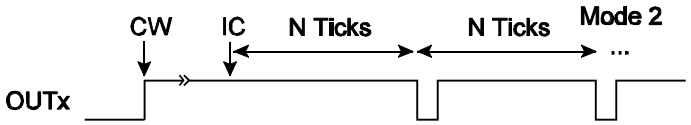
CONTROL WORD	SC1	SC0	RW1	RW0	M2	M1	M0	BCD
*STATUS WORD	OUT	CNT == 0	RW1	RW0	M2	M1	M0	BCD

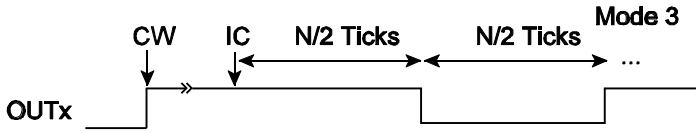
OPERATION MODES OF THE 82C54A

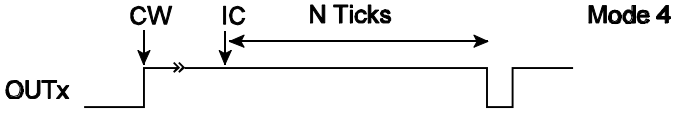
- Refer to the 82C206 data sheets in your Lab Manual.
- **CW** : Write control word.
- **IC** : Write count, N.
- **T** : External trigger at Gate input.











82C54A PROGRAMMING EXAMPLE

- Assume CLK0 is a 1.8432MHz clock.
- Write a procedure to generate a square-wave output at OUT0 with a period = T milliseconds.
- Assume T is passed as an unsigned word variable.
- NOTE: For Mode 3 operation the count loaded into the 8254A must be ≥ 2 to ensure proper counter operation.

```
#define  CNT0
#define  CNTCTL

void SQ_WAVE(unsigned T)
{
outportb(CNTCTL, 0x36);              // Program Counter-0 for
N.WRD = (18432 * T ) / 10 ;          // 16-bit, Mode-3 operation.
if (N.WRD >= 2 )  {
     outportb(CNT0, N.BYT.LSB) ;  // Load Counter-0 with 16-
     outportb(CNT0, N.BYT.MSB) ; // bit count, N.
     }
}
```

82C54A PROGRAMMING EXAMPLE (CONT'D)

"C" Data Structure for Byte / Word Access

```
union BW {
     stuct {
          char LSB ;
          char MSB ;
          } BYT ;
     unsigned WRD ;
     } ;
union BW N ;
```

Reading the count of an 82C54A Counter

- Write ***counter latch*** or ***read back*** command to the 82C54A control register then read the counter.

```
     outportb(CNTCTL, 0x00) ;        // Latch Counter-0.
     N.BYT.LSB = inportb(CNT0) ;     // Read Counter-0,
     N.BYT.MSB = inportb(CNT0) ;     // LSB then MSB.
```

REAL TIME CLOCKS

- Peripherals dedicated for maintaining year-month-day-hour-min-sec.
- Battery backed.
- Multiple alarms (interrupts) may be programmed.
- Example : MC146818

WATCHDOG TIMERS

- H/W circuit that activates its OP when its IP is not pulsed /adjusted within a certain interval of time.
- Like a re-triggerable one-shot.
- Used to detect certain types of computer failure.
- OP may be connected to the CPU Reset or NMI !
- Example : 82C54A operating in Mode 0.